

Notice of References Cited	Application/Control No. 10/010,238	Applicant(s)/Patent Under Reexamination BLATT ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,397,172	05-2002	Gurney, David J.	703/14
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Bogliolo et al., "Gate-Level Power and Current Simulation of CMOS Integrated Circuits" 1997 IEEE pg. 473-488.			
	V	Brown et al., "Overview of Complementary GaAs Technology for High-Speed VLSI Circuits" 1998 IEEE pg.47-51.			
	W	Bogliolo et al., "Node Sampling: a Robust RTL Power Modeling Approach" 1998 ACM pg.461-467.			
	X	Gupta et al., "Analytical Models for RTL Power Estimation of Combinational and Sequential Circuits" 2000 IEEE pg. 808-813.			

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.